U.S. **UTILITY** Patent Application

| O.I.P.E. | PATENT DATE |
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| SCANNED TR4 Q.A. 11 | |

| APPLICATION NO. | CONT/PRIOR | CLASS | SUBCLASS | ART UNIT | EXAMINER |
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| 09/877027 | F | ~~257~~ | | 2811 | |

APPLICANTS: Yasuhiko Tsukikawa

TITLE: Configuration for generating a clock including a delay circuit and method thereof

PTO-2040
12/99

## ISSUING CLASSIFICATION

| ORIGINAL | | CROSS REFERENCE(S) | |
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| CLASS | SUBCLASS | CLASS | SUBCLASS (ONE SUBCLASS PER BLOCK) |
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| INTERNATIONAL CLASSIFICATION | | | |
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| ☐ TERMINAL DISCLAIMER | DRAWINGS | | | CLAIMS ALLOWED | |
|---|---|---|---|---|---|
| | Sheets Drwg. | Figs. Drwg. | Print Fig. | Total Claims | Print Claim for O.G. |
| ☐ The term of this patent subsequent to _____ (date) has been disclaimed. | _____ (Assistant Examiner) _____ (Date) | | | NOTICE OF ALLOWANCE MAILED | |
| ☐ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ | _____ (Primary Examiner) _____ (Date) | | | ISSUE FEE | |
| | | | | Amount Due | Date Paid |
| ☐ The terminal ____months of this patent have been disclaimed. | _____ (Legal Instruments Examiner) _____ (Date) | | | ISSUE BATCH NUMBER | |

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